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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,814	01/12/2004	Takeshi Sakata	NITT.0173	1567

7590 06/21/2005

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/754,814	SAKATA ET AL.
	Examiner	Art Unit
	Thong Q. Le	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,8-14 and 16-19 is/are rejected.

7)☒ Claim(s) 7,15 and 20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 01/12/2004.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

> by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-6,8-14,16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Makuta et al. (U.S. Patent No. 6,480,415).

Regarding claim 1, Makuta et al. disclose a semiconductor device (Figure 1), comprising:

a non-volatile memory cell array including a plurality of word lines, plurality of bit lines intersected with the a plurality of word lines, and a plurality of non-volatile memory cells arranged at respective positions where the a plurality of word lines are intersected with the a plurality of bit lines (Column 7, lines 5-27);

a write buffer (31) for supplying a write signal corresponding to write data;

an input buffer (30) for supplying the write data write buffer; and

a write data register (15) connected to the input buffer and holding the write data (Column 7, lines 16-20).

Regarding claims 2-6, Makuta et al. disclose an address register (12) for holding an address input from external; and a comparator (Figure 9, 60) for comparing an address held in the address register with an input address (Column 17, lines 6-14);

wherein the semiconductor device outputs the write data held in the data register the comparator indicates that the address held the address register agrees with the input address (Column 8, lines 6-15, Column 17, lines 15-23), and wherein the comparator makes a comparison at subsequent read access after write is done to the non-volatile memory cell array (Column 17, lines 6-48), and wherein if the comparator indicates that the address register agrees with the input address, the semiconductor device performs no read operation from the non-volatile memory cell array (Column 8, lines 20-38), and a sense amplifier block which supplies read voltage to a selected bit line of the lines in the read operation; wherein the sense amplifier block does supply the read voltage the comparator indicates that the address held the address register agrees with the input plurality of bit address (Figure 1, 15), and address transition detector which detects an address transition (Column 8, lines 20-38).

Regarding claims 8-14,16-19, Makuta et al. disclose a semiconductor device, comprising: a memory cell array including a plurality of word lines, a plurality lines which are intersected with the a plurality of word lines, and a plurality of memory cells which are arranged at respective positions where the a plurality of word lines are intersected with the a plurality of bit lines (Figure 1, Column 7, lines 5-27); a write buffer (31) for supplying a write signal corresponding to write data; an input buffer (30) for supplying the write data to the write buffer; a write data register (15)connected to the input buffer and holding the write data; and a flag register (STR) for holding a flag, wherein the flag indicates whether the write data held the write data register valid (Column 7, lines 30-45), and wherein the flag register set by a write operation (WE), and wherein the flag

register is reset when the semiconductor device is powered on (Column 7, lines 30-67), and wherein the flag register reset when a desirable period of time has lapsed after the write operation (Column 30-67), and an address register (12) for holding an address input from external; and comparator for comparing an address held in the address register with the next input address; wherein the comparator performs the comparing operation if the flag indicates the write data is valid and does not perform the comparing operation if the flag indicates the write data is invalid (Column 17, lines 25-48), and an address transition detects an address transition detector which semiconductor device (Column 8, lines 20-38).

Allowable Subject Matter

8. Claims 7,15,20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7,15,20 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Makuta et al. (U.S. Patent No. 6,480,415), and others, does not teach the claimed invention having a non-volatile memory cells each have a phase change resistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER